Amendments to the Specification:

In paragraph [0002]:

The present invention relates to a laser-power control ~~laser-powercontrol~~ apparatus employed in an optical recording device. More particularly, a power-control device for ~~devicefor~~ an optical disc recording system that controls the optical power stably during high-speed optical information recording even if using a relative low-speed front photodiode is disclosed.

In paragraph [0004]:

A laser diode is usually used as a light source in a conventional optical recording apparatus. It is well known that the optical power output of a laser diode varies greatly with changes in environmental temperature. Accordingly, it is necessary to ~~compensatefor~~ compensate for unwanted temperature-induced power fluctuations in the operation of laser diodes. A feedback control device for stabilizing the output power of a laser diode is called an automatic power control (APC) and is ~~generallyutilized~~ generally utilized in a conventional optical recording apparatus.

In paragraph [0006]:

Fig.2 is a block diagram illustrating a prior art APC structure 10. In this figure, a laser diode LD radiates laser light onto an optical disc (not shown). The light radiated by the LD is received by a front photodiode FPD. The output of the FPD is converted into a voltage signal, front photodiode output ~~(FPDO)signal~~ (FPDO) signal, through a current-to-voltage conversion unit 20. The FPDO voltages corresponding to bias (read) power, erase power, and write ~~powerduring~~ power during reproduction and recording operations are respectively measured by a power level acquisition unit 30. The measured voltages are outputted by the power level acquisition unit ~~30as~~ 30 as $V_{b,m}$, $V_{e,m}$, and $V_{w,m}$. Feedback controller units 40, in accordance with the ~~individualdifferences~~ individual differences between the reference voltages $V_{b,r}$, $V_{e,r}$, and $V_{w,r}$ set by a reference power

level setting unit 50 and the measured voltages $V_{b,m}$, $V_{e,m}$, and $V_{w,m}$, output the required bias level, erase level, and write level currents into an LD driving unit 60 for producing desired recording pulses into the LD for recording information pits into the optical disc.

In paragraph [0007]:

To correctly measure the output power of a laser diode, a sample and hold circuit is usually employed in the power level acquisition unit 30 of a conventional optical recording ~~apparatus.Various~~ apparatus. Various sampling signals are issued according to the information data to be recorded and the corresponding write strategy. Then the voltage levels of the FPDO during the bias period, erase period, and write period are sampled and held for feedback control. Precise power control is thus obtained despite fluctuations in the temperature of the LD. Nevertheless, it is implicitly assumed, in the sample and hold scheme, that the response speed of the FPD is approximately the same as the modulation speed of the recording pulse of the LD. In other words, the FPDO must follow tightly the changes of each recording pulse of the ~~LDso~~ LD so that a sampling device can correctly sample the power levels of the LD from the FPDO. For example, as shown in Fig. 3, the time duration of the erase period in a rewritable optical disc format is ~~generallylong~~ generally long enough to allow the FPDO to closely approximate the recording pulse of the LD and provide a qualified sampling area for APC.

In paragraph [0008]:

In a high-speed and/or high-density optical recording application, the response speed ~~ofthe~~ of the FPD is likely to be slower than the modulation speed of the recording pulse of the ~~LD.This~~ LD. This results in the FPDO having only a short time period in steady state. This problem is illustrated in Fig. 4 where even though the FPDO response reaches steady state near the end of an erase period, a medium-speed sampling device may fail to correctly sample the desired FPDO value.

In paragraph [0009]:

Obviously, implementation of a high-response-speed sample and hold circuit is expensive. In certain recording ~~formatssuch~~ formats such as those using blue laser diodes, the recording pulse widths are so short that correctly sampling the FPDO is impossible for present hardware implementation technology under the constraint of reasonable costs. Additionally, as the recording pulses get shorter and shorter, it is very likely that the response speed of the FPD is much slower than the modulation speed of the recording pulse of the LD. As shown in Fig.5, the FPDO cannot correctly reflect the optical power output of the ~~LD.In~~ LD. In this situation, the real output power cannot be measured correctly even with the use of a perfect sample and hold ~~circuitregardless~~ circuit regardless of cost.

In paragraph [0011]:

One method employed in the power level acquisition unit 30 is to use a peak (or bottom) envelope detection device, which continuously tracks the peaks (or bottoms) of the FPDO for feedback control. Chuang, herein incorporated by reference, discusses such a device in U.S. Patent Application Publication US 2002/0141313. Here, peak envelope signals outputted from the envelope detection devices are fed to standard sample and hold circuits, which in turn, output to the respective feedback control ~~units.However,~~ units. However, to reliably detect and reflect peaks (or bottoms) of the FPDO, the discharge time constant of a peak (or bottom) envelope detection device cannot be too large compared to that of the recording pulses of the ~~LD.If~~ LD. If the discharge time constant is too large, the peak (or bottom) envelope detection device may not correctly follow the FPDO. If the discharge time constant is too small, output from the peak (or bottom) envelope detection device may incur small dropouts in the detected peak (or bottom) envelope in spite of the same amplitude for each peak (or bottom) in the FPDO shown in Fig.6.

In paragraph [0012]:

Additionally, when the response speed of the FPD is much ~~slowerthan~~ slower than the modulation speed of the recording pulse of the LD, the FPDO cannot achieve steady state within a recording pulse, and hence the output signal of a peak (or bottom) envelope detection device will also follow the variation due to write strategy, as shown in Fig.7. Since a peak (or bottom) envelope detection device will track the local maximum peaks existing in the inputted pulses train, the power measured by a peak (or bottom) envelope detection device will continuously change because of the write strategy when an FPD with low response speed is used. Since the acquired power deviations result from the write strategy and temperature drifts simultaneously, the feedback controller unit will perform wrong power adjustments because of erroneously sensed FPDO variations resulting from write strategy. Consequently, it will be difficult to stably compensate real power fluctuation resulting from the effect of temperature.

In paragraph [0014]:

A first embodiment of the present invention includes a peak-hold circuit and a sample and hold circuit. The peak-hold circuit has a first input for receiving a front photodiode (FPD) output pulse sequence (FPDO), a second input for receiving a reset signal from a control circuit, and an output for outputting a measured maximum voltage of the FPDO. The sample and hold circuit has a first input for receiving the output of the peak-hold circuit, a second input for receiving a sampling signal (SH) from the control circuit, and an output. In accordance with the difference between a ~~referencevoltage~~ reference voltage and the output of the sample and hold circuit, a feedback controller unit outputs the required current level into a laser diode (LD) driving unit for producing desired recording pulses into the LD for recording information pits into an optical disc.

In paragraph [0026]:

~~Figs.8-10are~~ Figs.8-10 are block diagrams of an Automatic Power Control according

to the present invention.

In paragraph [0030]:

~~Fig.15is~~ Fig.15 is a block diagram of another multi-pulse peak-hold circuit according to the present invention.

In paragraph [0032]:

~~Fig.17is~~ Fig.17 is a block diagram of another multi-pulse peak-hold circuit according to the present invention.

In paragraph [0034]:

~~Fig.19is~~ Fig.19 is a block diagram of another multi-pulse peak-hold circuit according to the present invention.

In paragraph [0035]:

The present invention proposes a multi-pulse peak-hold device in a power level acquisition unit, instead of using a high-speed sample and hold circuit such as those frequently adopted in a conventional optical recording apparatus. Fig.8 is a block diagram of the present invention if three power level controls are configured in an Automatic Power Control (APC) structure 110. Similar reference numerals are used for those components of the APC 110 that serve the same function as the corresponding components of the prior art APC 10. These functions have been previously described in this paper and will not be again elaborated on here. The ~~obviousdifferences~~ obvious differences in the present invention APC 110 from the prior art are the multi-pulse peak-hold (or bottom-hold) device 130 and the calibration gain 140 located in the output of the multi-pulse peak-hold (or bottom-hold) device ~~130thatis~~ 130 that is manifested in high-speed and/or high-density optical storage applications when a relatively low speed front photodiode (FPD) is used. The use of the calibration gain will be discussed later in

this application.

In paragraph [0038]:

It should be noted that a ~~forwardpath~~ forward path from the reference voltage setting unit 150 to the feedback controller unit 40 may be configured for the respective power level control in an APC structure to speed-up its transient response when operating from a reading state to a writing state in a conventional optical recording apparatus. Fig.10 is a block diagram showing the application of the present ~~invention190~~ invention 190 if forward paths 195 are added to each APC loop.

In paragraph [0041]:

~~Fig.12and~~ Fig.12 and Fig.13 contrast the action of the peak-hold circuit 210 with that of a prior art peak envelope circuit. In Fig.12, the response speed of the FPD is approximately the modulation speed of the recording pulse of the LD and the FPDO goes to steady state in each pulse. That is, the peaks in the FPDO pulses are equal in magnitude no matter what write strategy is used. A low-speed peak-hold circuit 210 can follow the peaks up after a certain number of pulses and hold it, as shown in Fig.12. Subsequently, a low-speed sample and hold circuit is satisfactory for sampling the real write power of the LD by an appropriate sampling signal SH. Namely, by using a low-speed peak-hold circuit 210 and a low-speed sample and hold circuit 220, the write power will be measured correctly. The result is superior to that of using the prior art peak envelope detection device in the power level acquisition unit 30, in the sense that the peak-hold circuit 210 of the present invention substantially avoids the slight dropout in the detected peak envelope as shown in Fig.12.

In paragraph [0043]:

Because there will be several equivalent highest peaks and a few peaks very close to the highest peaks within ~~thepredetermined~~ the predetermined time span, the MPHO will

approach them stably in the considered time span. The reason is briefly described here. The recording pulse train can be viewed as the superposition of many single recording pulses occurring in different timings and the FPDO is the superposition of the FPD response for each single recording pulse.

In paragraph [0044]:

It is noted that the FPD response for a single recording pulse of short period will go to zero after a certain time duration. For example, consider a relatively low-speed FPD with time constant 2T receiving a recording pulse with a 0.5T pulse width ~~ata~~ at a point 20T before the next recording pulse, where T is the period of the channel bit clock for the considered optical storage application. For simplicity, only first-order response is taken into account here for a low-speed FPD. It can then be approximated mathematically that less than 0.003% of the FPD response of the considered recording pulse will remain at the starting point of the next recording pulse that is 20T away. That means that only those recording pulses within several channel bits before the next recording pulse will contribute to any significant degree to the FPD response at the starting point of the next recording pulse, which can be regarded as the initial condition of the FPD response for the next recording pulse.

In paragraph [0045]:

Because the combined patterns by the recording pulses for a short time, e.g. 20T, are limited and will repeat many times within a certain time span, close initial conditions occur many times within that span. Accordingly, the FPD response of each next recording pulse ~~dependsgreatly~~ depends greatly on the width of that next pulse and the initial condition and also results in many ~~responsessimilar~~ responses similar in amplitude within a certain time span because of finite pulse widths and combined patterns. Hence it is expected that the FPDO gets several equivalent highest peaks and a few peaks very close to the highest peaks within a certain time span, and MPHO will be held almost fixed after

a short time interval in the considered time span by a low-speed peak-hold circuit.

In paragraph [0046]:

Fig.14 is a diagram illustrating the operation of the multi-pulse peak-hold device 200 if an FPD with low response speed is used. In this optical storage example, the steady state of the FPDO in the erase period is so short that it is inconvenient for power sampling. However, the write power can still be acquired via the peak-hold circuit 210 employed in the multi-pulse peak-hold device 200. The sampling signal SH is issued to sample the MPHO in a frequency much lower than that of the recording pulses because the bandwidth requirement of the APC response is low. The time span necessary ~~forthe~~ for the MPHO to come to a stable state can be experimentally determined. The reset signal is issued after the sampling signal SH goes low to clear the MPHO and to re-initialize the action of the peak-hold circuit 210. The output of the multi-pulse peak-hold device 200 is $V_{w,m}$ which is maintained approximately constant if there is no temperature drift. As a result, a low-speed sample and hold ~~circuit220~~ circuit 220 is capable of acquiring the maximum value of the FPDO during high-speed and/or high-density optical storage applications.

In paragraph [0049]:

Similarly, a low-speed bottom-hold circuit can also be used in the multi-pulse peak-hold ~~device200~~ device 200 to hold the minimum value of the bottoms in the FPDO. A low-speed sample and hold circuit 220 is also capable of acquiring the bias power for low-speed optical storage applications or that of the minimum value in the FPDO for high-speed and/or high-density optical storage applications even though an FPD with relative low response speed is employed.

In paragraph [0052]:

An obvious difference in the multi-pulse peak-hold device ~~300from~~ 300 from the

multi-pulse peak-hold device 200 is the addition of the switch 340 controlling the transmission of the FPDO to the peak-hold circuit 310 according to a control signal "window" from the encoding unit 330. The window signal may select random sequences from the FPDO pulse train. The feasibility of selecting random FPDO sequences is similar to that of the first embodiment of the present invention 200 because the MPHO, after a certain time interval, comes to a stable value for random FPDO sequences. The width of the window signal (the time span) can be experimentally determined. The window signal may also select a predetermined FPDO sequence according to fixed recording data patterns. The example of selecting a FPDO pulse sequence with predetermined recording data patterns will be discussed later.

In paragraph [0053]:

In a case where the response speed of the FPD is ~~approximatelythe~~ approximately the same as the modulation speed of the recording pulse of the LD, the FPDO goes to steady state in each pulse. Therefore, the use of the switch 340 and window signal can be effectively omitted and the present implementation can easily function similarly to that of Fig.11 by maintaining an active window signal and setting the sampling signal SH in Fig.11 as the logical AND operation of the two signals, SH and window, in Fig. 15.

In paragraph [0054]:

In a case where the response speed of the FPD is slower than the modulation speed of the recording pulse of the LD, e.g. in high-speed recording, the FPDO may only very briefly attain a steady state within each recording pulse or even worse the FPDO may never attain a steady state, as previously discussed. Accordingly, the peaks of the FPDO are much likely to be fluctuant, not always correctly indicating the real LD power level. Through the use of a window signal, only those recording data patterns that make local maximum peaks or attain values near local maximum peaks in the FPDO sequence need be considered. As a result, the MPHO will attain a stable ~~value.For~~ value. For example,

the special combination of the longest bias (erase) period and the shortest writing period, corresponding to a data pattern of the longest land and the shortest pit, usually produces a maximum or a near fixed FPDO value because the longest bias (erase) period will result in close initial conditions for the following recording pulse and the shortest write period often starts with the widest recording pulse. The window signal can be enabled at the start of that pattern and can be disabled at the end of the pattern.

In paragraph [0055]:

Though the response speed of the peak-hold circuit adopted is much slower than that of the FPDO, the MPHO may achieve maximum after several window signals. Then a low-speed sample and hold circuit at low-cost is qualified for sampling the MPHO. After sampling, a reset signal is used to re-initialize the peak-hold circuit. Fig.16 illustrates the operation of the multi-pulse peak-hold device 300 when a relatively low-speed FPD is used. In this optical storage example, the steady state of the FPDO in the erase period is so short that it is inconvenient for power sampling. ~~Thusthe~~ Thus the window signal is issued to sift the pattern consisting of the longest erase period and the shortest write period.

In paragraph [0059]:

If only one power level must be measured in an APC structure, only one peak-hold or one bottom-hold circuit is needed in the multi-pulse peak-hold device 300 to obtain the required power level. The other power level can be referred from the measured power level. Fig.17 illustrates an implementation of an APC structure 400 where only the write power level is measured because the write power has a better Signal to Noise Ratio (SNR) than the erase power. The bias power is controlled by an open-loop control method, i.e. the reference power level setting unit 150, via a digital to analog converter 480, sets the bias level current directly. The write power is precisely controlled with a feedback controller unit 40 by means of a multi-pulse peak-hold device 130 embedded in the loop.

Since it is reasonable to assume that a linear relationship exists between the power and the current for an ~~LDwhen~~ LD when the current exceeds its threshold level, the erase power is nearly fixed proportionally to the write power. Consequently, if the write power is accurately measured, the erase power can be referred to from the write power by multiplying it with a proportional constant 485 C_e. As a result, the erase power can be controlled by such a pseudo-closed loop method.

In paragraph [0061]:

It should noted that the MPHO may be different from the real optical power output of the laser diode due to insufficient FPD response speed as shown in Fig.14 and Fig.16. However, precise output power control of the LD can be realized via a proper calibration procedure. In the following paragraphs, a calibration approach is ~~disclosedthat~~ disclosed that may be used in the present invention.

In paragraph [0062]:

Fig.18 shows an identification procedure for obtaining a calibration gain G, i.e. the inverse of the ratio of the measured power to the real power. This identification procedure may be performed before the optimal power calibration (OPC) procedure that is used to determine the optimal recording power for a specified recording speed. Additionally, ~~ifthe~~ if the identification procedure is executed under the condition of de-focus so that the light intensity of the LD is greatly reduced in the focal region, the test write power will not impair the optical storage medium. The identification procedure comprises two steps: Step 1 measures the voltage level Y_1 of the FPDO using LD recording pulses with a time duration long enough to allow the MPHO to closely reflect the maximum real power; step 2 measures the voltage level Y_2 under normal LD recording pulses. Obviously reversing the order of performing steps 1 and 2 are intended to fall within the scope of the present invention.

In paragraph [0065]:

Once the voltage values Y_1 and Y_2 have been obtained, there are at least two ways to properly calibrate the APC of the present invention. A first way is to increase the output of the peak-hold circuit by multiplying the output of the peak-hold circuit with a proportional constant to compensate for the difference from real LD output power. Therefore, the calibration ~~gainG_x~~ gain G_x in Fig.8 can be determined as being equal to the inverse of Y_2/Y_1 which represents the response capability of the FPD under the specified recording speed. If the response speed of the FPD ~~isapproximately~~ is approximately the same as the modulation speed of the recording pulse of the LD, G_x approximately equals "1". G_x becomes larger if the response speed of the FPD ~~becomesslower~~ becomes slower than the modulation speed of the recording pulse of the LD.

In paragraph [0066]:

A second way is to reduce the output of the reference power level setting unit 150 by multiplying the output of the reference power level setting ~~unit150~~ unit 150 with a proportional constant 505 and to maintain the input to the feedback controller unit 40 unchanged by multiplying the output ~~ofan~~ of an error amplifier 515 with another proportional constant 510. An alternative implementation as shown in Fig.19 can be thus constructed for achieving stable power control even a FPD with insufficient response speed is ~~used.Therefore,~~ used. Therefore, the calibration ~~gainG_x~~ gain G_x in Fig.19 can be determined as being equal to Y_1/Y_2 and the calibration gain K_x (proportional ~~constant505~~ constant 505) can be determined as being equal to Y_2/Y_1. After performing the identification procedure shown in Fig.18, the system controller will set the corresponding calibration gains G_x ~~andK_x~~ and K_x for each power level control loop in the APC structure 530. Consequently, precise power control for desired power levels can be achieved.

In paragraph [0067]:

Additionally, it is well known that the reference power level setting unit is

commanded by a system controller via power setting scripts in the firmware code. Therefore, the proportional constant K_x can be set directly in the firmware code by modifying the power command setting. For example, if the original power command is $P=P_w$, then it can be changed to $P=K_wP_w$. Accordingly, the hardware shown in ~~Fig.19for~~ Fig.19 for the calibration gain in the power level setting unit can be omitted.

In paragraph [0068]:

In contrast to the prior art, the present ~~inventionutilizes~~ invention utilizes a low-speed, peak-hold circuit to obtain, hold, and output a maximum of the FPDO. One example of the present invention uses a predetermined window signal or a plurality of window signals of a total duration long enough to allow the outputted MPHO to stabilize. After MPHO stabilization, an SH signal causes a low-speed and low-cost sample and hold circuit to sample and hold the outputted MPHO. When the MPHO has been sampled and held, a reset signal clears the outputted MPHO and reinitializes the peak-hold circuit. In accordance with the difference ~~betweena~~ between a reference ~~voltageand~~ voltage and the output of the sample and hold circuit, a feedback controller unit outputs the required current level into an LD driving unit for producing desired recording pulses into the LD for recording information pits into the optical disc.